What Is Claimed Is:

1. A memory device, comprising:

a digit line formed in a substrate;

a memory cell in electrical communication with said digit line;

a first conductive line in electrical communication with said memory cell; and

a second conductive line in electrical communication with said memory cell.

2. The memory device of claim 1, wherein said memory cell comprises a chalcogenide element.

3. The memory device of claim 1, wherein said first conductive line comprises a metal element.

4. The memory device of claim 1, wherein said second conductive line comprises a metal element.

5. The memory device of claim 1, wherein said digit line is overlaid with titanium silicide.

6. The memory device of claim 1, wherein said second conductive line is electrically coupled to said digit line at a plurality of contacts.

7. The memory device of claim 1, further comprising an electrical contact plug coupling said digit line to said second conductive line.

8. The memory device of claim 11, further comprising a plurality of said electrical contact plugs coupling electrically said digit line to said second conductive line.

9. A memory array, comprising:

a plurality of memory cells, each memory cell comprising a programmable resistive element and an access device coupled to said resistive element;

a digit line in electrical communication with said access devices; and

a strapping layer in electrical communication with said digit line at a plurality of locations.

10. The memory structure of claim 9, wherein a maximum distance between each of said ovonic devices is approximately equal to a minimum photolithographic limit.

11. The memory structure of claim 9, further comprising a first number of access devices coupled to said digit line, and a second number of locations at which said strapping layer is coupled to said digit line, wherein said second number is approximately one-half said first number.

12. A memory device, comprising:

a first conductive plug having a first type conductivity and having a width approximately equal to a minimum photolithographic limit;

a second conductive plug having a second type conductivity; and

an insulative spacer interposed between said first and said second conductive plugs wherein a total width of said second conductive plug and said spacer is approximately no greater than a minimum photolithographic limit.

13. A memory device, comprising:

two first conductive plugs having a first type conductivity distanced one from the other by a maximum distance approximately equal to a determined dimension;

a second conductive plug having a second type conductivity, said second conductive plus interposed between said two first conductive plugs; and

an insulative spacer interposed between said second conductive plug and said two first conductive plugs wherein a total width of said second conductive plug and said spacer is no greater than said determined dimension.

14. The memory-device of claim 13, wherein said determined dimension is representative of a minimum feature size for a selected photolithographic process.

15. A semiconductor device, comprising:

a plurality of diodes in electrical communication with a substrate;

a first digit line in electrical communication with said plurality of diodes; and

a strapping layer in electrical communication with said first digit line.

16. The semiconductor device of claim 15, further comprising a plurality of contacts electrically coupled between said first digit line and said strapping layer.

17. The semiconductor device of claim 15, further comprising a second digit line physically between said first digit line and said strapping layer.

18. A method for making a memory device, comprising the steps of:

providing a substrate having a first conductive line therein;

forming a plurality of diode access device memory cells in electrical communication with said first conductive line;

forming a second conductive line, said second conductive line in electrical communication with one of said memory cells; and

forming a third conductive line in electrical communication with said first conductive line and said plurality of memory cells.

19. A method for making a memory device, comprising the steps of:

providing a substrate having a first conductive line therein;

forming a plurality of memory cells, each said memory cell comprising an element programmable to multiple states of resistance;

forming a second conductive line, said second conductive line in electrical communication with one of said memory cells; and

creating a third conductive line in electrical communication with said first conductive line and said plurality of memory cells.

20. A method for forming a memory array, comprising the steps of:

forming a digit line in a substrate;

forming a plurality of memory cells in a first insulative layer, said memory cells overlying said digit line and in electrical communication with said digit line, each memory cell comprising an element having an alterable resistance, said first insulative layer having an opening therein;

forming a contact plug in said opening, said plug in electrical communication with said digit line;

forming a plurality of first conductive lines disposed with one of said first conductive lines overlying and in electrical communication with a selected one of said memory cells; and

forming a second conductive line in a second conductive layer, said second conductive line in electrical communication with said contact plug.

21. The method of claim 20, wherein said step of forming said plurality of memory cells further comprises the steps of:

forming a plurality of diodes in said insulative layer, said diodes in electrical communication with said digit line; and

forming a plurality of programmable devices coupled with each of said diodes in electrical communication with a corresponding one of said elements of alterable resistance.